

FIG. 1

0002/0" 2003/03/05

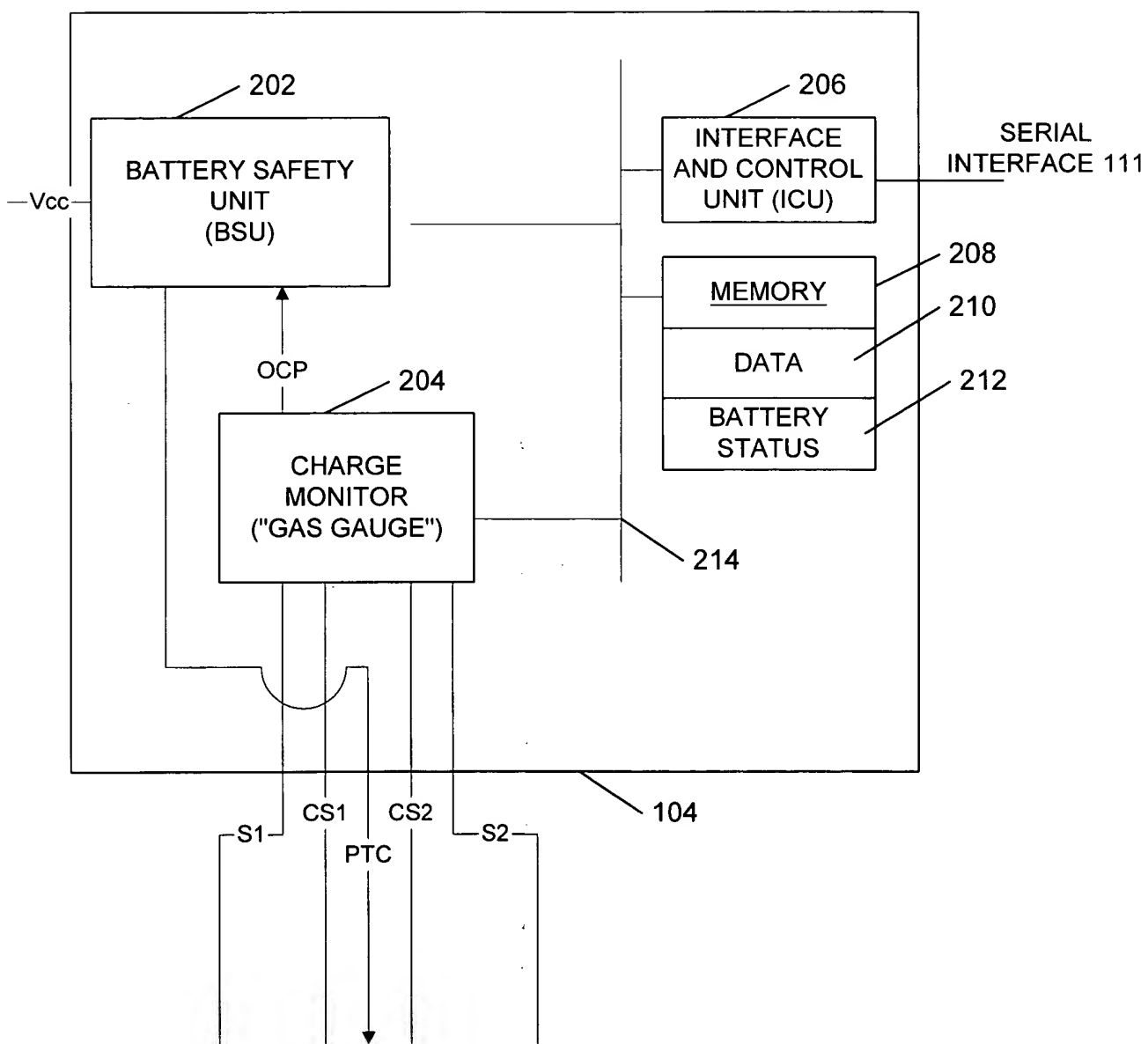


FIG. 2

The diagram shows a differential amplifier circuit. The top section, labeled 301, contains two input buffers (306, 308) and two comparators (CMP1, CMP2). The bottom section, labeled 311, contains a counter (318) and a logic gate (316). The circuit is connected to a feedback capacitor (310) and a common source (204). The input signals are VB1, VB2, and VB3. The output is OCP. The circuit is divided into two main sections by a dashed line, labeled 301 and 311. The top section (301) contains a differential amplifier with inputs VB1 and VB2, and a feedback capacitor CM. The bottom section (311) contains a counter (318) and a logic gate (316). The circuit is connected to a common source (204) and a feedback capacitor (310). The input signals are VB1, VB2, and VB3. The output is OCP.

**FIG. 3**



504

START

506

ACK

508

ONE

510

ZERO

FIG. 5

000240 80603960

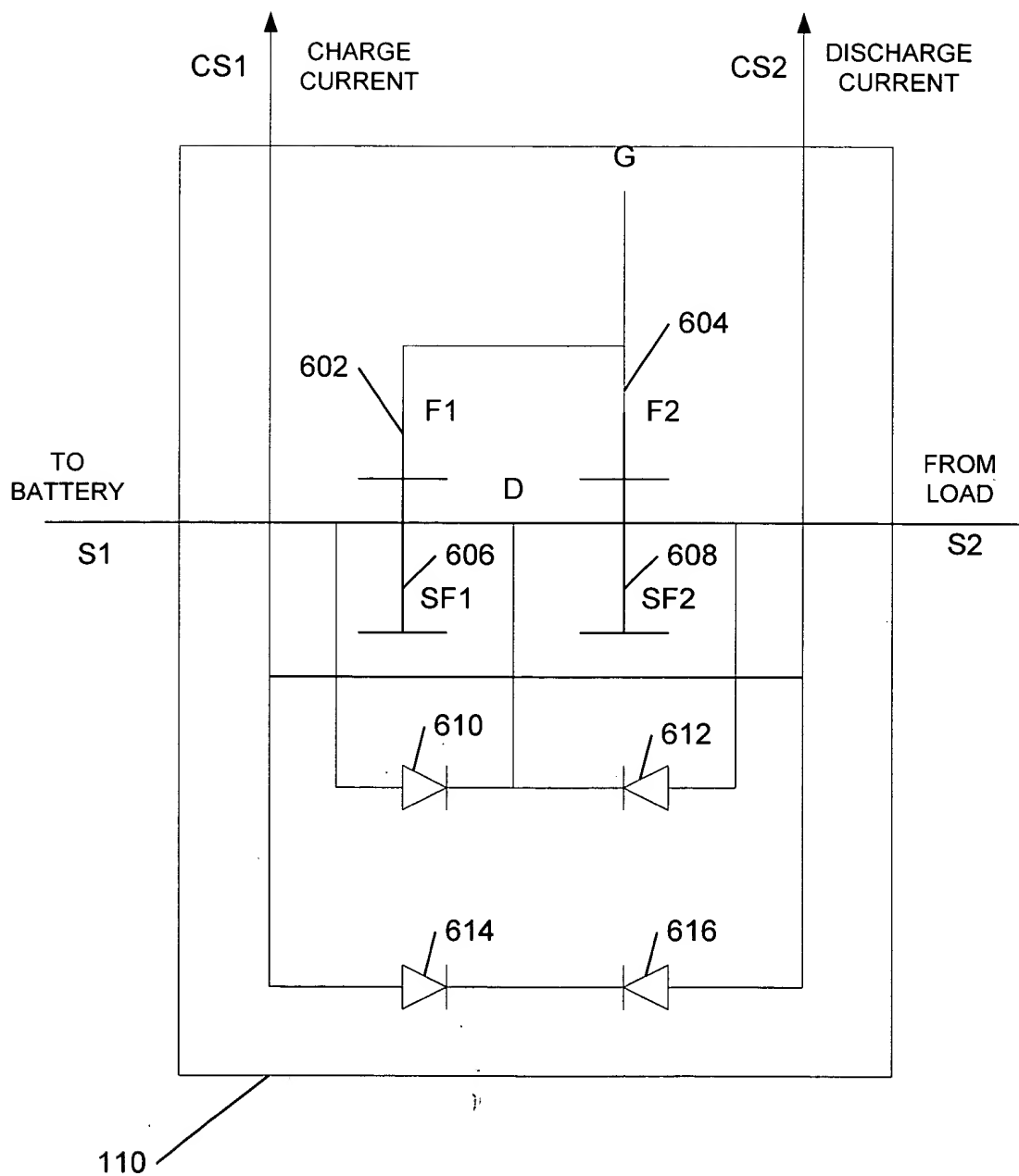


FIG. 6